Adaptiv Runtime R pairable Entry Register Fil

ABSTRACT OF THE DISCLOSURE

Methods and apparatus are disclosed that provide for improved addressing of a register file in a computer system. The register file has one or more redundant words. A logical address in an instruction is mapped, during a predecode operation, to a physical address having a larger address space than the logical address. Addresses of nonfaulty words are mapped to the same word in the larger address space as the logical address. Logical addresses that point to faulty words are mapped to a redundant word that is in the larger address space but not in the address space of the logical address. Because all addresses presented to a register file decoder at access time point to nonfaulty words, no delay penalty associated with address compare during the access time is required.